UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/913,859 | 03/28/2002 | Gregory J. Momber | SIEBE96517-US | 5466 |

23626 7590 02/09/2005

LEYDIG VOIT & MAYER, LTD
6815 WEAVER ROAD
SUITE 300
ROCKFORD, IL 61114-8018

| EXAMINER | |
|---|---|
| SQUIRES, BRETT S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/913,859 | MOMBER, GREGORY J. | |
| | Examiner | Art Unit | |
| | Brett S Squires | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

### *Drawings*

1. The corrected drawings submitted by the amendment received on November 15, 2004 are accepted by the examiner.

### *Specification*

2. The changes made to the specification by the amendment received on November 15, 2004 are accepted by the examiner.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-11 and 13-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Pecore (US 6,014,325).

Pecore discloses a controlled transformerless DC power supply having dual outputs with the same polarity with respect to ground (figure 2, col. 5 lines 20-27, col. 7 lines 1-35) with the first DC output (figure 2 ref# 119) and a second DC output (figure 2 ref# 116). The diodes (figure 2 ref# 124,126,128,130) are used to shift the ac input 180 degrees for the second DC output (col. 6 lines 37-67 and col. 7 lines 1-17).

The first DC output (figure 2, ref# 119) has a diode rectifier (figure 2 ref# 124,126,128,130) with a regulated dc output exhibiting a first polarity and includes a voltage regulator having at least one Zener diode (figure 2 ref# 140). The second DC output (figure 2, ref# 116) has a diode rectifier (figure 2 ref# 124,126,128,130) with a regulated dc output inverted to the first polarity and includes a voltage regulator having at least one Zener diode (figure 2 ref# 134,136). The second dc output also includes an inverter having a common emitter transistor (figure 2 ref# 142 col. 7 lines 51-67, col. 8 lines 1-23).

Pecore further discloses the Zener diodes for each dc output are connected to a filter (figure 2 ref# 103,105, col. 5 lines 47-50 and 65-68).

Pecore even further discloses the controlled transformerless DC power supply has a relay voltage, which is controlled by a microprocessor (col. 4 lines 53-67 and col. 5 lines 1-7).

Regarding Claim 5:

Pecore discloses several types of switching devices may be used in place of the shown bipolar transistor (col. 8 lines 20-23). If an n-channel MOSFET is used in place of the bipolar transistor, it would have a common source.

Regarding Claim 9:

Pecore discloses a first and second Zener diode connected in series for the second voltage regulator (figure 2 ref# 134,136) and one Zener diode connected for the first voltage regulator. It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a second Zener diode connected in series for the first voltage regulator, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being obvious over Pecore (US 6,014,325) and Tanoi (US 5,498,991).

Pecore discloses the above stated controlled transformerless DC power supply having a microprocessor, but does not disclose the microprocessor is controlled by a level shifter circuit.

Tanoi discloses a level shifter circuit (abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included in Pecore the level shifter circuit such as that taught by Tanoi in order to ensure the control signals being sent from the sensors to the microprocessor are of the correct voltage levels. The motivation to include the level shifter circuit in the controlled transformerless DC power supply having a microprocessor is reduce the risk of the microprocessor being damaged by extremely high voltage signals and not being able to interpret extremely low voltage signals.

***Response to Arguments***

7. Applicant's arguments filed November 15, 2004 have been fully considered but they are not persuasive.

8. In response to applicant's argument that Pecore does not include an inverter connected to the second wave rectifier but rather includes a transistor connected to the second wave rectifier and applicant's argument that Pecore does not include means for inverting connected to the second means for voltage regulation. The examiner would first like to define what an inverter is:

Inverter – (electric power) a machine, device, or system that changes direct-current power to alternating-current power (IEEE. The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition.)

The applicant's invention has a direct current (dc) power supply unit ~~has with~~ having a transformerless capacitor arrangement for creating a first low voltage dc output and a second low voltage dc output from an alternating current (ac) power supply wherein the second dc output has the same polarity of the first dc output. The direct current provided by the second output is not inverted into alternating current and thus the applicant's transistor is not an inverter. In as much as the transistor disclosed by the applicant is an inverter, the transistor connected to the second dc output in Pecore (US 6,014,325) figure 2 ref# 142 is an inverter and is read on "inverter".

9. In response to applicant's argument that Pecore does not include a means for shifting the AC input 180 degrees for input into second means for rectifying. The examiner would first like to define what a phase shift is:

Phase Shift – the absolute magnitude of the difference between two phase angles.

1. The phase shift between two planes of a 2-port network is the absolute magnitude of the difference between the phase angles at those planes. The total phase shift or absolute phase shift, is expressed as the total number of cycles, including any fractional number, between the two planes, where one complete cycle is 2pi radians or 360 degrees. Relative phase shift is the total or absolute phase shift less the largest integral number of 2pi radians or 360 degrees. The unit of phase shift is, therefore, the radian

or the electrical degree. The term 2-port network is used in its most general sense to include structures of passive or active elements. This includes the case of a given length of waveguide but may also refer to any two ports of a multiport device, where it is understood that a signal is incident only at one port.

2. A phase shift can be either a phase lead (advance) or a phase lag (delay).

The applicant's invention has a direct current (dc) power supply unit has with a transformerless capacitor arrangement for creating a first low voltage dc output and a second low voltage dc output from an alternating current (ac) power supply wherein the second dc output has the same polarity of the first dc output. The applicant's invention does not provide for phase shifting, thus shifting the AC input 180 degrees for input into the second rectifying means, refers to rectifying the negative portion of the AC input signal into a positive DC output. This is disclosed by Pecore's controlled transformerless DC power supply having dual outputs with a positive polarity with respect to ground in figure 2.

10. In response to applicant's argument that there is no suggestion or motivation to combine Tanoi and Pecore, the examiner would like to point out that microprocessors are powered by a DC power sources of 1.8V-3.3V, thus a voltage of 24 volts being applied to a microprocessor would cause the microprocessor to overheat and damage the microprocessor.

***Conclusion***

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brett S. Squires whose telephone number is (571)272-2268. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brett S Squires
Examiner
Art Unit 2836

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800